What is claimed is:

1. A method of forming a thin film on an integrated circuit substrate including a stepped portion, the method comprising:

forming a spin on glass (SOG) film on the substrate including the stepped portion to fill a recess defined by the stepped portion;

soft baking the SOG film at a temperature of less than about 400°C;

etching the soft baked SOG film; and

forming an insulation film on the etched SOG film.

2. The method of Claim 1, wherein forming the SOG film comprises forming the SOG film using a SOG solution including polysilazane.

3. The method of Claim 1, wherein etching the soft baked SOG film is followed by thermally treating the SOG film at a temperature from about 400°C to about 1200°C to convert the etched SOG film to silicon oxide.

4. The method of Claim 3, wherein thermally treating the SOG film is performed before forming an insulation film on the etched SOG film.

5. The method of Claim 1, wherein etching the soft baked SOG film comprises etching the soft baked film to a height lower than the recess defined by the stepped portion and wherein forming an insulation film includes forming the insulation film on the etched SOG film to a height greater than the recess defined by the stepped portion.

6. The method of Claim 5, wherein etching the soft baked SOG film further comprises etching the SOG film to expose a surface of the stepped portion and wherein forming the insulation film further comprises forming the insulation film on the exposed surface of the stepped portion.

7. The method of Claim 1, wherein soft baking the SOG film is performed at a temperature from about 100°C to about 300°C.

8. The method of Claim 1, wherein etching the SOG film comprises wet etching the SOG film using a hydrogen fluoride (HF) solution.

9. The method of Claim 1, wherein the insulation film includes oxide and wherein forming the insulation film comprises forming the insulation film using a chemical vapor deposition (CVD) process.

10. The method of Claim 1, wherein etching the soft baked SOG film is followed by thermally treating the substrate.

11. The method of Claim 1, wherein the stepped portion includes a plurality of gate electrodes and metal wiring patterns and/or trenches formed on the substrate.

12. The method of Claim 1, further comprising planarizing the formed insulation film.

13. The method of Claim 12, wherein planarizing the formed insulation film comprises planarizing the formed insulation film using a chemical mechanical polishing (CMP) process.

14. A method of forming a trench isolation film including forming a thin film according to the method of Claim 1, wherein the stepped portion comprises a trench on the substrate, the method further comprising removing the formed insulation film to expose the substrate adjacent the trench.

15. A method of forming a trench isolation film on an integrated circuit substrate, the method comprising:

forming a trench on the substrate using a pattern;

forming a spin on glass (SOG) film on the substrate including the formed trench to fill the trench;

soft baking the SOG film at a temperature of less than about 400°C;

etching the soft baked SOG film;

forming an insulation film on the etched SOG film;

removing a portion of the formed insulation film to expose the pattern;

removing the exposed pattern; and

planarizing a remaining portion of the insulation film.

16. The method of Claim 15, wherein forming the SOG film is preceded by forming a liner on a surface of the substrate, a sidewall of the trench and/or a bottom face of the trench.

17. The method of Claim 15, wherein etching the soft baked SOG film is followed by thermally treating the etched SOG film at a temperature from about 400°C to about 1200°C to convert the etched SOG film to silicon oxide.

18. The method of Claim 15, wherein soft baking the SOG film is performed at a temperature from about 100°C to about 300°C.

19. The method of Claim 15, wherein etching the SOG film comprises wet etching the SOG film using a hydrogen fluoride (HF) solution.

20. The method of Claim 15, wherein the insulation film includes oxide and wherein forming the insulation film comprises forming the insulation film using a chemical vapor deposition (CVD) process.

21. The method of Claim 15, wherein planarizing a remaining portion of the insulation film comprises planarizing the remaining portion of the insulation film using a chemical mechanical polishing (CMP) process.

22. A method of forming a thin film on an integrated circuit substrate, the method comprising:

forming a spin on glass (SOG) film on the substrate;

soft baking the SOG film at a temperature of less than about 400°C;

etching the soft baked SOG film; and

forming an insulation film on the etched SOG film.

23. A method for forming a thin film comprising:

forming a spin on glass (SOG) film on a substrate including a stepped portion by coating an SOG solution on the stepped portion and on the substrate wherein the SOG film at least partially fills up a recess formed by the stepped portion;

soft baking the SOG film;

etching the SOG film; and

forming an insulation film on a resultant structure formed on the substrate.

24. The method of Claim 23, wherein the soft baking the SOG film is performed at a temperature of about 100°C to about 300°C.

25. The method of Claim 23, wherein the SOG film is etched by a wet etching process using a hydrogen fluoride (HF) solution.

26. The method of Claim 23, wherein the insulation film includes oxide and the insulation film is formed using a chemical vapor deposition (CVD) process.

27. The method of Claim 23, further comprising thermally treating the substrate including the resultant structure.

28. The method of Claim 27, wherein the substrate is treated at a temperature of about 400°C to about 1,200°C.

29. The method of Claim 23, wherein the stepped portion includes at least two gate electrodes, at least two metal wiring patterns or trenches formed on the substrate.

30. The method of Claim 23, further comprises planarizing the insulation film using a chemical mechanical polishing (CMP) process.

31. A method for forming a trench isolation film comprising:

forming a trench on a substrate by etching the substrate using a pad oxide film pattern and a hard mask pattern as etching masks;

forming an SOG film on a substrate to sufficiently fill up the trench by coating an SOG solution on the substrate including the trench;

soft baking the SOG film;

etching a whole surface of the SOG film;

forming an insulation film on a resultant structure formed on the substrate;

partially removing the insulation film to expose the hard mask pattern;

removing the hard mask pattern and the pad oxide film pattern; and

removing the insulation film remaining on a surface of substrate to expose the surface of the substrate.

32. The method of Claim 31, wherein the soft baking the SOG film is performed at a temperature of about 100 to about 300°C.

33. The method of Claim 31, wherein the SOG film is etched by a wet etching process using an HF solution.

34. The method of Claim 31, wherein the insulation film includes oxide and the insulation film is formed using a CVD process.

35. The method of Claim 31, further comprising thermally treating the substrate including the resultant structure at a temperature of about 400 to about 1,200°C.

36. The method of Claim 31, wherein removing the insulation film is performed using a CMP process.

37. The method of Claim 31, further comprising continuously forming a liner including an insulation material on the surface of the substrate, on a sidewall of the trench and on a bottom face of the trench.